Amendments to the Specification:

Please replace the paragraph, beginning at page 1, line 4, with the following rewritten paragraph:

The present invention relates to a digital signal transceiver for transmitting and receiving ~~s~~ a signal modulated with a digital signal.

Please replace the paragraph, beginning at page 4, line 3, with the following rewritten paragraph:

The frequency modulator ~~61A~~ 61 receives a digital signal through the modulation input port 61b, modulates a high-frequency signal with the digital signal, and outputs the frequency-modulated signal through the output port 61a.

Please replace the paragraph, beginning at page 6, line 21, with the following rewritten paragraph:

Fig. 1 is a block diagram of a digital signal transceiver 50 according to an exemplary embodiment ~~2~~ of the present invention. The transceiver 50 includes a frequency modulator 5, a power amplifier 4 connected to an output port 5a of the frequency modulator 5, an antenna switch 3 having one branch port 3b connected to an output port of the power amplifier 4, an antenna terminal 2 connected to a common port 3c of the antenna switch 3, a receiving filter 6 connected to another branch port 3a of the antenna switch 3, a high-frequency amplifier 7 connected to an output port of the receiving filter 6, a receiving mixer 8 having one input port ~~8a~~ 8b connected to an output port of the high-frequency amplifier 7, and an output terminal 9 connected to an output port of the receiver mixer 8. The receiving mixer 8 further has another input port ~~8b~~ 8a connected to an output port 5a of the frequency modulator 5. The frequency modulator 5 has a transmitting modulation input ports 5b for receiving a digital signal and an input port 5c for receiving a phase locked loop (PLL) control data. The frequency modulator 5 outputs a frequency-modulated signal which

is modulated directly with the digital signal received through the input port 5b has a frequency determined by the PLL control data received through the input port 5c. The output signal of the frequency modulator 5 includes a phase noise changeable between a transmitting mode and a receiving mode.

Please replace the paragraph, beginning at page 8, line 25, with the following rewritten paragraph:

Fig. 2 is a block diagram of the frequency modulator 5 in the digital signal transceiver 50 of the embodiment. The frequency modulator 5 includes a PLL circuit. A frequency divider 21 has an input port ~~21a~~ 21 for receiving the digital signal from the transmitter modulation input port 5a. A phase comparator 24 has an input port 24a for receiving a signal from the output port 21c and has another input port 24b for receiving a signal generated by a reference signal generator 22 and transferred through the frequency divider 23. The reference signal generator 22 and the frequency divider 23 forms a reference-signal generating unit 22A. A charge pump 25 receives a signal from an output port 24c of the phase comparator 24. A switch 26 of electron type has a common port 26a connected to the output of the charge pump 25. The switch 26 has one branch port 26b connected to a low-pass filter (LPF) 27. Another ~~brabch~~ branch port 26c of the switch 26 is connected to an LPF 28. Respective output ports of the LPFs 27 and 28 are connected to a voltage-controlled oscillator (VCO) 29, a variable-frequency oscillator. An output of the VCO 29 is connected to the output port 5a for outputting the modulated signal. The frequency modulator 5 includes a data input port 5c for receiving PLL controlling data. More particularly, the output of the VCO 29 is connected to another input port 21b of the frequency divider 21. The VCO 29 is controlled with the PLL controlling data from the data input port 5c.

Please replace the paragraph, beginning at page 12, line 18, with the following rewritten paragraph:

(4) The frequency divider 23 has the dividing rate 1/R, in which the "R" is determined to be larger than that in the receiving mode. Then, the reference signal for

phase comparison output from the frequency divider ~~5~~ 23 is compared in phase with a signal having a frequency lower than that in the receiving mode. Accordingly, a minimum frequency range by which a transition frequency is changed according to one bit of the data of the digital input signal, i.e., a minimum step frequency can be narrow, hence allowing a frequency deviation to be determined accurately.